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PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10082392	02/25/2002	438 257	1	2827	Zarabian

**APPLICANTS: Vaiyapuri Venkateshwaran;

**CONTINUING DATA VERIFIED:
THIS APPLICATION IS A DIV OF 09/767,446 01/23/2001

** FOREIGN APPLICATIONS VERIFIED:
SINGAPORE 200003005-4 09/01/2000

PG-PUB DO NOT PUBLISH ☐ | RESCIND ☐

Foreign priority claimed ☐ yes ☐ no
35 USC 119 conditions met ☐ yes ☐ no
Verified and Acknowledged Examiners's intials

ATTORNEY DOCKET NO
2269-4369.1US (99-1230.1)

TITLE : Dual LOC semiconductor assembly employing floating lead finger structure

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G
ISSUE FEE: Amount Due / Date Paid	Primary Examiner	DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAMER	PREPARED FOR ISSUE	Application Examiner

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